3/13/02

Examiner Lewis, AU2822, CP3-3B07

Re: 09/930,847

Attached are edited search results from the patent and nonpatent commercial databases.

Based on this, if more searching, refining, or explanation is needed, please let me know.

Thanks,
Jeff Harrison
306-5429
CP4-9C18

```
     FILE 'HCAPLUS' ENTERED AT 10:05:55 ON 13 MAR 2002
               S SILICON/CN

     FILE 'REGISTRY' ENTERED AT 10:05:56 ON 13 MAR 2002
L1             1 S SILICON/CN

     FILE 'HCAPLUS' ENTERED AT 10:05:56 ON 13 MAR 2002
L2        317820 S L1
L3         38742 S L2(L)(POLY OR POLYCRYST? OR CRYST?)
               E THIN FILM TRANSISTOR/CT
               E E4+ALL/CT
L4         14977 S E9 OR TRANSISTORS(L)(FILM OR THIN OR THINFILM OR ULTRATHIN)
L5          3770 S L3 AND (L4 OR TFT OR TFTS)
L6            53 S L5 AND (ULTRA OR ULTRATHIN OR ULTRATHINFILM)
L7            19 S L6 AND CHANNEL###
L8            10 S L7 AND GATE##
L9             5 S L5 AND (ULTRA OR ULTRATHIN OR ULTRATHINFILM)(6A)CHANNEL###
```

L8 ANSWER 10 OF 10 HCAPLUS COPYRIGHT 2002 ACS
AN 1992:118218 HCAPLUS
DN 116:118218
TI Low temperature polysilicon **TFTs** using solid phase crystallization of very thin films and an electron cyclotron resonance chemical vapor deposition **gate** insulator
AU Little, Thomas W.; Takahara, Kenichi; Koike, Hideki; Nakazawa, Takashi; Yudasaka, Ichio; Ohshima, Hiroyuki
CS TFT Res. Lab., Seiko Epson Corp., Suwa, 392, Japan
SO Jpn. J. Appl. Phys., Part 1 (1991), 30(12B), 3724-8
CODEN: JAPNDE; ISSN: 0021-4922
DT Journal
LA English
CC 76-3 (Electric Phenomena)
Section cross-reference(s): 75
AB Low temp. (T .ltoreq.600.degree.) polycryst. Si **thin film transistors** (poly-Si **TFTs**) were fabricated by solid phase crystn. (SPC) of amorphous Si **films** deposited by low pressure CVD. These **TFTs** are distinguished by the very **thin** nature of the **channel** Si layer (25 nm) and the use of an SiO2 **gate** insulator deposited by electron cyclotron resonance CVD. The present process eliminates the need for hydrogenation and produces mobilities greater than 20 cm2/V.s and on/off current ratios greater than 107.

L9 ANSWER 1 OF 5 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:867071 HCAPLUS
DN 136:94058
TI Comparison study of metal induced lateral crystallized and solid-phase crystallized polycrystalline silicon **thin film transistors** with different channel thickness
AU Jin, Zhonghe
CS Dept. of Information and Electronic Engineering, Zhejiang University, Hangzhou, 310027, Peop. Rep. China
SO Japanese Journal of Applied Physics, Part 1: Regular Papers, Short Notes & Review Papers (2001), 40(11), 6325-6326
CODEN: JAPNDE
PB Japan Society of Applied Physics
DT Journal
LA English
CC 76-3 (Electric Phenomena)
AB N- and P-type polycryst. silicon **thin film transistors** are fabricated with channel thickness of 30 nm and 100 nm by metal induced lateral crystn. and conventional solid-phase crystn. of amorphous silicon. Significant improvement is obtained for the metal induced lateral crystn. devices by **ultrathin channel** layer. However, for solid-phase crystn. devices, improvement is not as significant. The possible reasons are proposed and discussed.

13mar02 08:31:55 User259284 Session D1699.2

```
SYSTEM:OS  - DIALOG OneSearch
  File   2:INSPEC  1969-2002/Mar W2
         (c) 2002 Institution of Electrical Engineers
  File   6:NTIS  1964-2002/Mar W4
         (c) 2002 NTIS, Intl Cpyrght All Rights Res
*File   6: See HELP CODES6 for a short list of the Subject Heading Codes
(SC=, SH=) used in NTIS.
  File   8:Ei Compendex(R)  1970-2002/Mar W2
         (c) 2002 Engineering Info. Inc.
  File  34:SciSearch(R) Cited Ref Sci  1990-2002/Mar W2
         (c) 2002 Inst for Sci Info
  File 434:SciSearch(R) Cited Ref Sci  1974-1989/Dec
         (c) 1998 Inst for Sci Info
  File 144:Pascal  1973-2002/Mar W2
         (c) 2002 INIST/CNRS
  File  35:Dissertation Abs Online  1861-2002/Mar
         (c) 2002 ProQuest Info&Learning
  File  94:JICST-EPlus  1985-2002/Jan W4
         (c)2002 Japan Science and Tech Corp(JST)
*File  94: There is no data missing. UDs have been adjusted to reflect
 the current months data. See Help News94 for details.
  File  99:Wilson Appl. Sci & Tech Abs  1983-2002/Jan
         (c) 2002 The HW Wilson Co.
  File 350:Derwent WPIX  1963-2001/UD,UM &UP=200216
         (c) 2002 Derwent Info Ltd
*File 350: Price changes as of 1/1/02. Please see HELP RATES 350.
More updates in 2002.  Please see HELP NEWS 350.
  File 347:JAPIO  Oct/1976-2001/Nov(Updated 020305)
         (c) 2002 JPO & JAPIO
*File 347: JAPIO data problems with year 2000 records are now fixed.
Alerts have been run.  See HELP NEWS 347 for details.
  File 344:CHINESE PATENTS ABS  APR 1985-2001/Dec
         (c) 2002 EUROPEAN PATENT OFFICE

      Set  Items  Description
S1      45003   THRESHOLD()VOLTAGE? ?
S2      60382   LEAK????(N)CURRENT? ?
S3       2566   1AND2
S4       3840   S1 AND MOBILIT???
S5       2084   S2 AND MOBILIT???
S6        431   SOURCE(1W)DRAIN()TERMINAL? ?
S7      77804   (SOURCE OR DRAIN)(2N)CURRENT? ?
S8      14489   (SOURCE OR DRAIN)(2N)RESIST?????????
S9      31557   SELF()ALIGN??????
S10       810   ALIGN?????(2N)ITSELF
S11       679   SELFALIGN?
S12       106   NONSELF()ALIGN??????
S13        15   NONSELFALIGN?
S14       387   4AND5
S15     32707   S9:S13
S16         0   14AND6
S17        58   14AND7
S18         6   14AND8
S19        18   14AND15
S20         1   3AND6
S21        40   S1:S2 AND S6
S22         5   S21 AND (S4 OR S5 OR S7:S8 OR S15)
S23     41045   TFT OT TFTS OR (THINFILM? OR THIN()FILM? ? OR ULTRATHIN)(6-
```

```
            N)(TRANSISTOR? ? OR FIELD()EFFECT?? OR FET OR FETS)
S24          14   17AND23
S25           4   18AND23
S26          12   19AND23
S27           0   20AND23
S28           4   21AND23
S29           1   22AND23
S30          31   S20 OR S24:S29
S31          18   RD S30 (unique items)
S32        6723   S1:S21 AND S23
S33         336   S32 AND (ULTRATHIN???????? OR ULTRA()THIN?? OR ULTRA()THIN-
              FILM????)
S34           1   ULTRA()THINFILM????
S35         242   S33 AND GATE??
S36        4231   S32 AND GATE??
S37        2539   S32 AND CHANNEL???
S38        1758   36AND37
S39          49   S38 AND (SIDEWALL?? OR SIDE()WALL??)
S40         780   S38 AND (POLYSI OR POLYSILICON OR (POLYCRYST? OR POLY()CRY-
              ST?????? OR POLY)()(SI OR SILICON))
S41         302   S40 AND (CONDUCT???? OR ELECTRODE??)
S42           1   33AND39
S43           1   33AND41
S44           2   S42:S43
S45          27   33AND8
S46          21   S31 OR S34 OR S44
S47          27   S35:S41 AND S45
S48          34   S46 OR S30
S49          26   S47 NOT S48
S50          17   RD S49 (unique items)
S51          60   S47:S50
S52          14   39AND40
S53          14   52AND38
S54          14   53AND41
S55          14   S54 NOT S51
S56          14   RD S55 (unique items)
```

44/9/2 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013646982 **Image available**
WPI Acc No: 2001-131191/200114
XRPX Acc No: N01-097311
MOS type **thin-film transistor** has thin **polycrystalline silicon** film in **channel** area to which laser irradiation is provided to increase crystallinity of **gate electrode**
Patent Assignee: NEC CORP (NIDE)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2000349293	A	20001215	JP 99157051	A	19990603	200114	B

Priority Applications (No Type Date): JP 99157051 A 19990603
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2000349293	A		7	H01L-029/786	

Abstract (Basic): JP 2000349293 A
NOVELTY - The **channel** (6) has thin film of **polycrystalline-silicon** to provide crystallinity to **gate electrode** (4) through **gate** oxide film (5). By laser irradiation to **polycrystalline silicon**, improvement in crystalline is achieved. The source (2) and drain (3) are linked to **channel**. Crystal degradation portion (7) is provided on reverse side of **gate electrode** in **channel**.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for manufacturing method of MOS type **thin-film transistor**.
USE - For MOS type **thin film transistor**.
ADVANTAGE - Since the crystal degradation portion of the **ultrathin** film is on reverse side of **polycrystalline-silicon** thin film, suppresses homogeneously the raise in minority carrier concentration in **channel** near the source, thereby suppressing the pressure-**resistance** reduction between **source** and drain.
DESCRIPTION OF DRAWING(S) - The figure shows top view and mid sectional view of the MOS type **thin film transistor**.
Source (2)
Drain (3)
Gate electrode (4)
Gate oxide film (5)
Channel (6)
Crystal degradation portion (7)
pp; 7 DwgNo 1/4

31/9/8 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04715978 E.I. No: EIP97063686690
Title: Novel **self-aligned** polycrystalline silicon **thin-film transistor** using silicide layers
Author: Ryu, Jai Il; Kim, Hyun Churl; Kim, Sung Ki; Jang, Jin
Corporate Source: Kyung Hee Univ, Seoul, South Korea
Source: IEEE Electron Device Letters v 18 n 6 Jun 1997. p 272-274
Publication Year: 1997
CODEN: EDLEDZ ISSN: 0741-3106
Language: English
Document Type: JA; (Journal Article) Treatment: T; (Theoretical); X; (Experimental)
Journal Announcement: 9707W5
Abstract: A novel **self-aligned** polycrystalline silicon (poly-Si) **thin-film transistor** (TFT) was fabricated using the three layers of poly-Si, silicon-nitride, and thin amorphous silicon. Gate and source/drain silicide formation was carried out simultaneously following silicon nitride and amorphous silicon patterning, enabling the use of only two mask steps for the TFT. The fabricated poly-Si TFT using laser annealed poly-Si exhibited a field-effect **mobility** of 30.6 cm**2/Vs, **threshold voltage** of 0.5 V, subthreshold slope of 1.9 V/dec., on/off current ratio of approximately 10**6, and off-state **leakage current** of 7.88 multiplied by 10** minus **1**2 A/ mu m at the drain voltage of 5 V and gate voltage of minus 10 V. (Author abstract) 14 Refs.
Descriptors: **Thin film transistors**; Polycrystalline materials; Amorphous silicon; Silicon nitride; **Leakage currents**; Semiconductor device manufacture; Gates (transistor); Current voltage characteristics

31/9/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

6303352 INSPEC Abstract Number: B1999-09-2560R-022
Title: Polysilicon **thin-film transistors** using **self-aligned** cobalt and nickel silicide source and drain contacts
Author(s): Sarcona, G.T.; Stewart, M.; Hatalis, M.K.
Author Affiliation: Aspect Technol., Sunnyvale, CA, USA
Journal: IEEE Electron Device Letters vol.20, no.7 p.332-4
Publisher: IEEE,
Publication Date: July 1999 Country of Publication: USA
CODEN: EDLEDZ ISSN: 0741-3106
SICI: 0741-3106(199907)20:7L.332:PTFT;1-L
Material Identity Number: I338-1999-007
U.S. Copyright Clearance Center Code: 0741-3106/99/$10.00
Language: English Document Type: Journal Paper (JP)
Treatment: Applications (A); Practical (P); Experimental (X)
Abstract: Polysilicon **thin-film transistors** (TFTs) with island thickness of 20 and 70 nm were fabricated with **self-aligned** cobalt and nickel silicide contacts to the source and drain. The silicide contacts are shown to reduce the series resistance, which limits the on-current of the device, thus significantly increasing the effective **mobility** in the 20-nm island devices. The **mobilities** of 20-nm cobalt and nickel silicided devices are similar to those with 70-nm islands, 31 versus 33 cm/sup 2//V-s, whereas the nonsilicided 20-nm devices have a **mobility** of only 13 cm/sup 2//V-s. The island thickness is shown to influence other device parameters affecting active matrix display driver circuit design, such as **threshold voltage**, **leakage current**, and subthreshold swing; all these parameters are improved when the island thickness is decreased. (6 Refs)
Subfile: B
Descriptors: carrier **mobility**; cobalt compounds; elemental semiconductors; **leakage currents**; nickel compounds; semiconductor device metallisation; silicon; **thin film transistors**

50/9/5 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC

4817753 INSPEC Abstract Number: B9412-2560R-113
Title: Recess **channel** structure for reducing **source/drain** series **resistance** in **ultra-thin** SOI MOSFETs
Author(s): Chan, M.; Assaderaghi, F.; Parke, S.A.; Yuen, S.S.; Chenming Hu; Ko, P.K.
Author Affiliation: Dept. of Electr. Eng. & Comput. Sci., California Univ., Berkeley, CA, USA
p.172-3
Publisher: IEEE, New York, NY, USA
Publication Date: 1993 Country of Publication: USA xi+188 pp.
ISBN: 0 7803 1346 1
U.S. Copyright Clearance Center Code: 0 7803 1346 1/93/$3.00
Conference Title: Proceedings of 1993 IEEE International SOI Conference
Conference Sponsor: IEEE Electron Devices Soc
Conference Date: 5-7 Oct. 1993 Conference Location: Palm Springs, CA, USA
Language: English Document Type: Conference Paper (PA)
Treatment: New Developments (N); Practical (P)
Abstract: A new Recess-**Channel** technology has been developed which significantly reduces the **source/drain** series **resistance**. This technology is potentially very useful for **ultra-thin**-film fully depleted SOI MOSFET fabrication with arbitrary silicon film thickness. Silicide technology may also be used in conjunction with the Recess-**Channel** technique to further reduce the **source/drain** series **resistance** and increase the current drive. (3 Refs)
Subfile: B
Descriptors: insulated **gate** field effect transistors; semiconductor technology; semiconductor-insulator boundaries; silicon; **thin film transistors**

50/9/6 (Item 6 from file: 2)
DIALOG(R)File 2:INSPEC

4655316 INSPEC Abstract Number: B9406-2560R-039
Title: Recessed-**channel** structure for fabricating **ultrathin** SOI MOSFET with low series resistance
Author(s): Chan, M.; Assaderaghi, F.; Parke, S.A.; Hu, C.; Ko, P.K.
Author Affiliation: Dept. of Electr. Eng. & Comput. Sci., California Univ., Berkeley, CA, USA
Journal: IEEE Electron Device Letters vol.15, no.1 p.22-4
Publication Date: Jan. 1994 Country of Publication: USA
CODEN: EDLEDZ ISSN: 0741-3106
U.S. Copyright Clearance Center Code: 0741-3106/94/$04.00
Language: English Document Type: Journal Paper (JP)
Treatment: Practical (P); Experimental (X)
Abstract: A new recessed-**channel** SOI (RCSOI) technology has been developed for fabricating **ultrathin** SOI MOSFET's with low **source/drain** series **resistance**. Thin-film fully depleted SOI MOSFET's with **channel** film thickness of 72 nm have been fabricated with the RCSOI technology. The new structure demonstrated a 70% reduction in **source/drain** series **resistance** compared with conventional processes. In the deep-submicron region, more than 80% improvement in saturation **drain current** and transconductance over conventional devices was achieved using the RCSOI technology. The new technology would also facilitate the use of silicide for further reducing the series resistance. (10 Refs)
Subfile: B
Descriptors: insulated **gate** field effect transistors; integrated circuit technology; MOS integrated circuits; semiconductor-insulator boundaries; silicon; **thin film transistors**

56/9/10 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

06244983 **Image available**
SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

PUB. NO.: 11-186557 [JP 11186557 A]
PUBLISHED: July 09, 1999 (19990709)
INVENTOR(s): HOTTA MASAYOSHI
APPLICANT(s): SHARP CORP
APPL. NO.: 09-353880 [JP 97353880]
FILED: December 22, 1997 (19971222)
INTL CLASS: H01L-029/786; H01L-021/336

ABSTRACT

PROBLEM TO BE SOLVED: To provide a **thin-film transistor** with improved switching characteristics having an on-current larger than that of the prior art by improving the drive capability of the transistor.

SOLUTION: In a transistor, a **channel** region 51 for a **polysilicon** thin film is arranged vertically so as to be positioned on a **sidewall** of a lower **gate electrode** 3a, and to surround the **electrode** 3a. Thus, the transistor has a double **gate** structure of the lower **gate electrode** 3a increasing the **channel** width and of an upper **gate electrode** 8a formed in a **side wall** shape, so as to surround the lower **electrode** 3a **self-alignedly** via **gate** insulating films 4 and 6.

56/9/9 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009488379 **Image available**
WPI Acc No: 1993-181914/199322
XRPX Acc No: N93-139865
Thin film FET mfr. for CMOS inverter - having **gate electrode** with overlying thin film **channel**, **gated** through insulator on top and **sidewalls** of **gate**
Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)
Inventor: MANNING M
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5214295	A	19930525	US 92827287	A	19920128	199322	B

Priority Applications (No Type Date): US 92827287 A 19920128
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5214295	A		12	H01L-027/01	

Abstract (Basic): US 5214295 A

The method, forming a **thin film field effect transistor** on a semiconductor substrate, involves forming a transistor **gate**, on the semiconductor substrate, the **gate** having a top surface and **sidewalls**. Sacrificial insulating spacers are formed on the **sidewalls** and the underlying substrate doped to form a MOSFET. A thin **gate** insulating layer is provided over the transistor **gate**, coating the transistor **gate** top surface and **sidewalls**, and with a thickness which is less than about 700 Angstroms.

A thin semiconductor film is formed over the transistor **gate** to a selected thickness, having a conductively doped thin film **channel** region and conductively doped thin film active regions. The thin film **channel** region contacts the thin **gate** insulating layer opposite the transistor **gate** top surface and opposite the **sidewalls**. The transistor **gate sidewalls** in operation **gate** the opposite thin film **channel** region through the thin **gate** insulating layer.

ADVANTAGE - **Self-aligned thin film transistor** with increased effective **gate** length only two **polysilicon** layers required for CMOS inverter.

Dwg.10/11
Title Terms: THIN; FILM; FET; MANUFACTURE; CMOS; INVERTER; **GATE**;

56/9/13 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO

04090850 **Image available**
MANUFACTURE OF **THIN FILM TRANSISTOR**

PUB. NO.: 05-082550 [JP 5082550 A]
PUBLISHED: April 02, 1993 (19930402)
INVENTOR(s): KITAJIMA HIROSHI
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 03-243378 [JP 91243378]
FILED: September 24, 1991 (19910924)
INTL CLASS: [5] H01L-021/336; H01L-029/784; H01L-021/265
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)
JAPIO KEYWORD: R097 (ELECTRONIC MATERIALS -- Metal Oxide Semiconductors, MOS); R100 (ELECTRONIC MATERIALS -- Ion Implantation)
JOURNAL: Section: E, Section No. 1407, Vol. 17, No. 415, Pg. 104, August 03, 1993 (19930803)

ABSTRACT

PURPOSE: To reduce a **leakage current** in a transistor and to make it possible to obtain uniform transistor characteristics by a method wherein silicon ions are implanted in the parts other than a part, which comes into contact to a **gate electrode** via a **gate** insulating film, of a silicon thin film to turn the parts of the silicon thin film into an amorphous film and the amorphous regions are crystallized by a heat treatment.

CONSTITUTION: A **thin film transistor** is manufactured via a silicon ion implantation process and a heat treatment process. The silicon ion implantation process is a process wherein silicon ions 310 are implanted in the parts other than a part in contact with an upper **gate electrode** 303 via a **gate** insulating film (a **gate** oxide film) 304, of a silicon thin film (a **polycrystalline silicon** substrate) 305 for forming a **channel** of the **thin film transistor** and the parts of the **thin film** 305 are brought into an amorphous state. Moreover, the heat treatment process is a process for crystallizing amorphous regions 311 by a heat treatment. After that, phosphorus ions are ion-implanted using the **electrode** 303, for example, as a mask and after **sidewalls** 316 are respectively formed on the end parts of the **electrode** 303, arsenic ions 315 are ion implanted.

56/9/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010085077 **Image available**
WPI Acc No: 1994-352790/199444
XRPX Acc No: N94-277027
Thin film transistor using crystalline and **polycrystalline silicon@** - incorporates **channel** domain without impurity extended to form offset domains as thick **side walls** to hold **gate electrode**
Patent Assignee: KAWASAKI STEEL CORP (KAWI)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 6275835	A	19940930	JP 9358949	A	19930318	199444	B

Priority Applications (No Type Date): JP 9358949 A 19930318
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 6275835	A		5	H01L-029/784	

Abstract (Basic): JP 6275835 A

The **thin film transistor** is manufactured on a silicon substrate (10). An insulating layer (11) adheres to the substrate while a **polycrystalline silicon** layer (12) is formed on the insulating layer (12). A **gate electrode** (14) is attached to a **gate** oxide film (13) above the **channel** domain (32).

The offset domains (33) extend on ether side of the **channel** domain to facilitate growth of source domain (30) and a drain domain (31) on either side of the polycrystalline semiconductor layer.The **electrodes** are be taken from the source and drain domain and these three **electrodes** forms the terminals for **thin film transistor**. Polycrystalline layer (12) is also provided.

ADVANTAGE - Prevents **leakage current**. Improves conductivity by controlling thickness of polycrystalline layer.

Dwg.1/4

56/9/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010343747 **Image available**
WPI Acc No: 1995-245835/199532
XRPX Acc No: N95-190900
Thin film transistor having lightly doped drain and offset structure for suppressing **leakage current**, for LCDs - has barrier layer comprising a metal different from that of **gate electrode**, and metal oxide layer comprises oxide of **gate electrode** metal
Patent Assignee: SAMSUNG ELECTRONICS CO LTD (SMSU)
Inventor: LEE J
Number of Countries: 003 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5430320	A	19950704	US 93168178	A	19931217	199532	B
JP 7226515	A	19950822	JP 93332174	A	19931227	199542	
KR 9710685	B1	19970630	KR 9322946	A	19931030	199946	

Abstract (Basic): US 5430320 A

Thin film transistor includes an insulating substrate,

a **polysilicon** layer comprising source and drain regions, a **channel** region formed between the source and drain regions, an impurity doped region formed between the source and **channel** regions and between the drain and **channel** regions, a **gate** insulating layer formed on the **polysilicon** layer, and a **gate electrode** formed on the **gate** insulating layer over the **channel** region.

The **gate electrode** comprises a metal, a metal oxide layer formed on the **sidewalls** of the **gate electrode** over the impurity doped region and a barrier layer formed on the **gate electrode**.

The impurity-doped region has a lower impurity concentration than that of the source and drain regions. The **gate electrode** metal has an oxide formed so as to extend outwardly during oxidation of the **sidewall** surface portion of the **gate electrode** for forming the metal oxide layer.

ADVANTAGE - Generation of a **leakage current** is prevented to improve operation stability, reproducibility is excellent and linewidth of TFT may be reduced ti improve brightness.

56/9/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011470130 **Image available**
WPI Acc No: 1997-448037/199741
Related WPI Acc No: 1996-517891
XRAM Acc No: C97-142850
XRPX Acc No: N97-373399

Thin film transistor with **self aligned** bottom **gate** - formed without the use of masks along the **sidewalls** of **gate electrode**

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: HSU L L; SACCAMANGO M J; SHEPARD J F
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5663578	A	19970902	US 95559809	A	19951117	199741	B
			US 96690882	A	19960802		

Priority Applications (No Type Date): US 95559809 A 19951117; US 96690882 A 19960802
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5663578	A		7	H01L-029/786	Div ex application US 95559809 Div ex patent US 5573964

Abstract (Basic): US 5663578 A

A **thin film transistor** comprises: a dopant source layer on top of a substrate; a doped **gate electrode** overlying and in contact with the dopant source layer; a **gate** insulator overlying and in contact with the **gate electrode**; an insulating **sidewall** spacers with at least two sides and a bottom, with the bottom in contact with the dopant source layer, and one side adjacent and in contact with at least the **sidewalls** of the **gate electrode** and **gate** insulator; a **polysilicon** body layer, having a doped source, a doped drain, a **channel** and an off-set regions where the source and drain regions are overlying and in contact with the dopant source layer, the **channel** region is overlying and in contact with the **gate** insulator, the off-set regions in contact with the **sidewall** spacer.

ADVANTAGE - Low cost process providing improved yield and reliability; **self aligned** process forms source and drain regions, and **self aligned** off-set regions; usable on large substrates and small cell size.

Dwg.3D/4

56/9/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011020941 **Image available**
WPI Acc No: 1996-517891/199651
Related WPI Acc No: 1997-448037
XRAM Acc No: C96-162594
XRPX Acc No: N96-436450

Thin film transistor on a substrate with an insulating surface layer - using diffusion from a dopant source layer to form a **self-aligned** bottom **gate**

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC); IBM CORP (IBMC)
Inventor: HSU L L; SACCAMANGO M J; SHEPARD J F
Number of Countries: 003 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5573964	A	19961112	US 95559809	A	19951117	199651	B
TW 304306	A	19970501	TW 96107709	A	19960626	199730	
KR 97030910	A	19970626	KR 9641758	A	19960923	199828	
KR 225231	B1	19991015	KR 9641758	A	19960923	200110	

Priority Applications (No Type Date): US 95559809 A 19951117
Abstract (Basic): US 5573964 A

Making a TFT comprises:

(a) providing a substrate with an insulating layer on top;

(b) forming a dopant source layer containing dopants on the insulating layer;

(c) forming a first layer of **polysilicon** on top of the dopant source layer;

(d) forming a layer of **gate** insulator on the **polysilicon**;

(e) patterning the **polysilicon** and the **gate** insulator to form a **gate** stack consisting of a **gate electrode** and **gate** insulator of the TFT;

(f) forming a **sidewall** spacer adjacent to and in contact with the **gate** stack on top of the dopant source layer;

(g) forming a second layer of **polysilicon** so as to be on top and in contact with exposed surfaces of the **gate** stack, and the dopant source layer;

(h) patterning the second layer of **polysilicon** to form a **channel** region, off-set regions, source and drain regions of the TFT;

(i) heating to diffuse the dopants from the dopant source layer into the source, drain regions and the **gate electrode** of the TFT.

USE - Fabrication of a **thin film transistor**.

ADVANTAGE - Low cost, improved yield and reliability; **self-aligned** source and drain regions and **self-aligned** off-set regions; simultaneous impurity doping of the **gate**, source and drain regions; usable on large substrates and can provide small cell size.

Dwg.3D/4

56/9/11 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

05440708 **Image available**
THIN FILM TRANSISTOR AND ITS MANUFACTURE

PUB. NO.: 09-055508 [JP 9055508 A]
PUBLISHED: February 25, 1997 (19970225)
INVENTOR(s): YAMADA TSUTOMU
JINNO MASASHI
HIRAI KYOKO
APPLICANT(s): SANYO ELECTRIC CO LTD [000188] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 07-204605 [JP 95204605]
FILED: August 10, 1995 (19950810)
INTL CLASS: [6] H01L-029/786; H01L-021/336; G02F-001/136
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components); 29.2 (PRECISION INSTRUMENTS -- Optical Equipment); 44.9 (COMMUNICATION -- Other)
JAPIO KEYWORD: R004 (PLASMA); R011 (LIQUID CRYSTALS); R100 (ELECTRONIC MATERIALS -- Ion Implantation)

ABSTRACT

PROBLEM TO BE SOLVED: To prevent that, at the time of etching a **poly silicon gate** in a p- SiTFT, defects are generated in a **gate** insulating film, and a **leak current**, avalanche deterioration, etc. occur from a carrier trap.

SOLUTION: A source region 11S and a drain region 11D which have high concentration are formed. Inside them, an LD region 11L of low concentration is formed. Further inside the LD region 11L, a VLD region 11VL of very low concentration is formed. Thereby electric fields on both end portions of a **channel** are relieved, so that generation of a **leak current** and avalanche deterioration is prevented. By covering the **side wall** of a **gate electrode** 13 with a spacer 14, and implanting impurity ions in the LD region 11L, the VLD region 11VL is formed in the manner in which the shadow part of the spacer 14 is doped with a very low concentration.

56/9/12 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

04299592 **Image available**
MANUFACTURE OF **THIN FILM TRANSISTOR**

PUB. NO.: 05-291292 [JP 5291292 A]
PUBLISHED: November 05, 1993 (19931105)
INVENTOR(s): MATSUMURA MITSUYOSHI
APPLICANT(s): CASIO COMPUT CO LTD [350750] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 04-116757 [JP 92116757]
FILED: April 10, 1992 (19920410)
INTL CLASS: [5] H01L-021/336; H01L-029/784
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)
JAPIO KEYWORD:R004 (PLASMA); R097 (ELECTRONIC MATERIALS -- Metal Oxide Semiconductors, MOS); R100 (ELECTRONIC MATERIALS -- Ion Implantation)
JOURNAL: Section: E, Section No. 1504, Vol. 18, No. 77, Pg. 166, February 08, 1994 (19940208)

ABSTRACT

PURPOSE: To easily obtain a fine and high precision off-set length in a **thin film transistor** having an off-set **gate** structure.

CONSTITUTION: A **side wall** 5a is formed at a **gate electrode** 4 by plasma CVD method and a source/drain region 6 is formed to a **poly-silicon** layer 2 by ion implantation with this **side wall** 5a and the **gate electrode** 4 used as the mask. The source/drain region 6 is formed on the **poly-silicon** layer 2 at the outside of the **side wall** 5a and the length of the **channel** region 7 projected to the outside of the **gate electrode** 4, namely the off-set length is determined by the width of the **side wall** 5a. The fine **side wall** 5a by plasma CVD method can be formed with excellent uniformity and reproducibility by forming a film on the entire surface by the plasma CVD method and thereafter etching this film with anisotropic dry etching method. Accordingly, a fine offset length can easily be formed with high accuracy on the **self-alignment** basis.

13mar02 10:35:40 User259284 Session D1700.2

SYSTEM:OS - DIALOG OneSearch
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Archive data (1986-2/99) is available in File 810.
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*File 613: File 613 now contains data from 5/99 forward.
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Set	Items	Description
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S2	0	S1 AND (THIN OR ULTRATHIN OR ULTRATHINFILM)(6N)CHANNEL??
S3	181	(POLY OR POLYCRYST? OR POLYSI?)(3N)CHANNEL??
S4	1903	(THIN OR ULTRATHIN OR ULTRATHINFILM)(6N)CHANNEL??
S5	11	3AND4
S6	0	1AND4
S7	0	1AND3
S8	8	RD S5 (unique items)

8/9/1 (Item 1 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

05221855 Supplier Number: 47964566 (THIS IS THE FULLTEXT)
Polysilicon TFTs could rival single-crystal silicon -- Laser anneal shows promise

Robinson, Gail
Electronic Engineering Times, p34
Sept 8, 1997
ISSN: 0192-1541
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 809

TEXT:

Livermore, Calif. -- By examining the process that uses a laser to recrystallize the **polysilicon channel** area when making **thin**-film transistors (TFTs), researchers have uncovered some surprising results that may significantly improve TFTs and give them higher mobility and lower threshold voltage.

When fabricating polysilicon TFTs, the order in which the active area of the device is recrystallized with an excimer laser has typically been considered arbitrary. But recent reports that have compared the order of the processes have shown significant differences in grain structures that can lead to differences in device performance. By fabricating thin-film transistors in pre-patterned laser recrystallized polysilicon films-where the active area is patterned first-researchers at Lawrence Livermore National Laboratories (LLNL) have reported increases in field-effect mobility of a factor of three, a reduction in threshold voltages from 5.3 to 0.007 V, and a halving of the subthreshold slope for W/L = 10 micrometer/10 micrometer TFTs.

"This represents the tip of the iceberg of the study for these types of devices," said Gary Guist, who did preliminary research at Arizona State University under Tom Sigmon, who is currently pursuing the research at LLNL. "This was the first work to study the difference between the patterned and unpatterned methods. It turns out that, depending on the order of the process, you get two very different types of grain structure."

Zones created

The unpatterned process starts off with a blanket silicon film that is recrystallized with a laser, then the active area is formed. The second process patterns the silicon film into the active area and is then also recrystallized. Comparison results have shown, in the prepatterned films, that multiple-pulsed laser irradiation at certain energy densities produced three well-defined zones containing different microstructures. "Previous experiments have shown obscure photos that made it difficult to pick out any grain boundaries," said Guist. "But at LLNL, the TEM lab images showed three different grain regions within the prepatterned film." A subsequent rework of the process based on that revelation confirmed that the grains correlate with the device performance, leading to better transistors in terms of device performance.

"The lab is currently developing the concepts more thoroughly-not necessarily work on low-temperature glass, but other substrates as well," said LLNL's Sigmon.

The new breakthrough could address the growing interest in very-high-performance polysilicon thin-film transistors for flat-panel displays. "Currently, a number of Japanese companies are interested in a system on glass, where not only is the display on glass, but also the electronic driver circuits," Sigmon said. "Also, they plan to have memory, processors and everything else right on the panel. So all of the electronics will be right on the glass itself."

But to get there, a very-high-performance thin-film transistor will be required. Sigmon started the excimer-laser process in the mid-1980s for

an ultra-shallow junction required for scaling FETs to smaller dimensions. The work gave him the background and equipment to pursue the current research in TFTs. "No one was interested in thin-film displays at that time," he said. "There is a lot of work going on, but not a lot of interest in the excimer-laser approach."

Sigmon saw the laser approach as being more efficient. "Why crystallize an entire panel? You etch off 99 percent of the silicon so that you are left with a very small amount that is actually the active transistor," he said. With the new approach, the silicon is patterned first and then selectively scanned with the laser. This results in lower costs and a faster turnaround of panels. But after mastering the process, Sigmon began to find clues to the current high-performance approach.

"What was interesting is that smaller patterns have larger grains when they regrow, and these larger grains give you higher-performance electrical characteristics," he said. That led to the idea of making little islands that are almost all large grain. If the grain boundaries and their direction can be controlled with respect to the transistor direction, it is possible to get very-high-performance transistors approaching single-crystal performance.

High mobility

In some of the work, not yet published, Sigmon will report electron mobility about 500 cm2 per volt-second-which approaches that of a regular silicon-on-insulator device. The next step in the research is to address uniformity problems. If these issues are resolved satisfactorily, the process could be ideal for flat-panel TFT pixel switches. "It would also be good for the driver and decoder circuits that people want to put on the panels; right now they are putting them on flip-chip," he said.

Sigmon pointed out that companies in Japan have already committed to excimer-laser processing for polysilicon TFTs. Toshiba Corp. recently announced a 12.3-inch diagonal panel that uses laser recrystallization. "We don't really have that technology here, but there is equipment available now and there is one U.S. manufacturer of some of the laser equipment," he said.

PUBLISHER NAME: CMP Publications, Inc.

8/9/2 (Item 2 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

03144346 Supplier Number: 44292952 (THIS IS THE FULLTEXT)
Devices Surfacing At IEDM May Duel In Next Century
Electronic News (1991), p1
Dec 13, 1993
ISSN: 1061-9577
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 983
TEXT:
WASHINGTON - At the International Electronic Devices Meeting here last week, semiconductor vendors showcased experimental devices that may someday become mainstream - including Hitachi's single-electron memory device, Texas Instruments' flat panel display and quantum effect devices, Toshiba's 0.04 micron gate electrode and AT&T's low-power 0.1-micron fabrication technology.

Hitachi said it has fabricated a prototype of a single-electron memory device operating at room temperature. To make the device, Hitachi said it used **thin** -wire **poly**-Si transistors; **channel** and gate were patterned with electron-beam lithography. Gate width and the gate length were 100nm while the gate oxide thickness is 150nm.

Hitachi said a major challenge was reducing capacitances of the active region in order to satisfy read/retention conditions. The 4nm thick **channel poly**-Si with 10nm lateral grain size was formed by amorphous silicon deposition followed by 750 deg C crystallization. 'In this process, the lateral crystallization is automatically suppressed after the vertical crystallization reaches the film thickness. Because there is a grain size variation in the channel, the electrons can flow only in a narrow energy creek within the channel when it is operated at low-current,' the Hitachi paper stated.

As a result, 'the effective channel width is narrowed to 10nm. A low-energy grain isolated from the current path acts as a storage node. The entire channel and gate are surrounded by SiO2, which further reduces all the capacitances.'

Hitachi said the device holds promise for a memory chip storing up to 16 billion bits and 'portable multimedia device application.' Researchers from Hitachi's Central Research Laboratory in Kokubunji, Japan, said 'From now on, single-electron devices should not be the research topic only of physicists. Rather we expect this work will encourage the serious research activity toward single-electron ULSIs.'

Texas Instruments said it has developed several ICs using quantum-mechanical effects that operate at room temperature. The company said previous devices based on quantum effects were limited to operations at -320 degrees F.

TI's Central Research Laboratories developed the new quantum effect chip using resonant tunneling transistors. The circuits are comprised of both co -integrated resonant tunneling bipolar transistor (RTBTs) and double heterojunction bipolar transistors (DHBTs) based on III-V heteroepitaxy on InP substrates. The quantum effect chips are projected to operate over three times faster and hold three times more functions than conventional chips.

TI said it used the resonant tunneling transistor technology to build a 3 -transistor XNOR, a 7-transistor XOR, a 5-transistor CARRY and a 17 -transistor full adder IC. Each circuit operates at 3V.

'Future generations of ICs will utilize resonant tunneling transistors. This opens up the possibility for smaller computers that operate faster than computers using today's technology. Practical applications of quantum devices are about five to six years away,' said Gary Frazier, nanoelectronics manager at TI. 'Demonstrating this circuit at

room temperature is a significant breakthrough for the practical, and near-term, utilization of quantum effect devices. They can be designed into commercial systems without the need for special cooling.'

AT&T Bell Laboratories reported fabricating a device with 0.1 micron dimensions which can operate at room temperatures. The experimental devices require only 1.5V to operate, compared with the 2.7V to 5V needed by most devices available today. Using regular silicon, Bell Labs was able to produce the devices with a new process it calls 'vertical doping.'

The silicon-based doping process enables the devices to function at frequencies up to 116 GHz for N-channel MOS and 51 GHz for P-channel. Previous records for cooled 0.1 micron geometries were 90 GHz for N-channel and 23 GHz for P-channel, according to AT&T.

The vertical doping concept was tested using Bell Labs CAD tools called Padre and Prophet. AT&T said it is working to apply the 1.5V power requirement for that geometry to larger design rules.

Toshiba Corp. reported it has developed a 0.04 micron gate electrode that it says opens the door to the fabrication of 100-Gbit memory IC chips and high -speed microprocessors. However, actual products based on the technology will probably not appear for 10 years.

Toshiba researchers implemented the electrode in a metal oxide semiconductor (MOS) transistor that the company claims is 40 percent smaller than any MOS transistor built to date. Normal operation of the transistor has been confirmed at normal room temperature, Toshiba officials said. 'We have especially high expectations that this technology will enable the production of super-high-speed microprocessors,' a Toshiba spokesman said.

Among the other IEDM developments were several papers describing flat panel technology in development. TI, for example, described the status of its Digital Micromirror (EN, Feb.8) and revealed that the contrast ratio of the DMD technology has been improved to 100:1. TI said this was necessary for it to become competitive with cathode ray tubes (CRTs).

The DMD is a reflective spatial light modulator technology consisting of an array of rotable aluminum mirrors. The DMD mirrors are fabricated over a six transistor SRAM cell using and 0.8 micron CMOS twin-well process. TI said SRAM cells were chosen because of their immunity to photo upset caused by light leakage into the address circuitry.

TI said it has thus far developed both single-chip and three-chip DMD devices; a 768x576 pixel array DMD was shown generating a direct-view image. TI also described a three-chip 768x576 projection TV creating a 13-ft. diagonal screen.

According to TI, each SRAM cell controls the state of rotation of the overlying mirror. A '1' in the memory cell causes the mirror to rotate plus 10 degrees; a '0' in the memory cell causes the mirror to rotate minus 10 degrees. Because of the fast switching speed of the mirrors, pulsewidth modulation can be used to achieve gray scale.

Among new papers for process technology for IC fabrication, Matsushita described 'damage-free metal etching using Lissajous electron plasma (LEP).' Matsushita said LEP is a low-pressure plasma source that does not use magnetic enhancement.

PUBLISHER NAME: Cahners Publishing Company

8/9/7 (Item 3 from file: 484)
DIALOG(R)File 484:Periodical Abs Plustext

03146789 (THIS IS THE FULLTEXT)
A silicon single-electron transistor memory operating at room temperature

Guo, Lingjie; Leobandung, Effendi; Chou, Stephen Y
Science (GSCI), v275 n5300, p649-651, p.3
Jan 31, 1997
ISSN: 0036-8075 JOURNAL CODE: GSCI
DOCUMENT TYPE: Feature
LANGUAGE: English RECORD TYPE: Fulltext; Abstract
WORD COUNT: 2221

ABSTRACT: A single-electron memory, in which a bit of information is stored by one electron, is demonstrated at room temperature. The structure and fabrication of the memory should be compatible with future ultralarge-scale integrated circuits.

TEXT:

Headnote:

A single-electron memory, in which a bit of information is stored by one electron, is demonstrated at room temperature. The memory is a floating gate metal-oxide-semiconductor transistor in silicon with a channel width (~10 nanometers) smaller than the Debye screening length of a single electron and a nanoscale polysilicon dot (~7 nanometers by 7 nanometers) as the floating gate embedded between the channel and the control gate. Storing one electron on the floating gate screens the entire channel from the potential on the control gate and leads to (i) a discrete shift in the threshold voltage, (ii) a staircase relation between the charging voltage and the shift, and (iii) a self-limiting charging process. The structure and fabrication of the memory should be compatible with future ultralarge-scale integrated circuits.

To increase the storage density of semiconductor memories, the size of each memory cell must be reduced. A smaller memory cell also leads to faster speeds and lower power consumption. One of the widely used nonvolatile semiconductor memories is the metal-oxide-semiconductor (MOS) transistor that has a floating gate between the channel and the control gate. Information is represented by storing charges on the floating gate. The information can be read by using the transistor because different amounts of charge on the floating gate shift the threshold voltage of the transistor differently. The ultimate limit in scaling down the floating gate memory is to use one electron to represent a bit, the so-called single electron MOS memory (SEMM). To make such memory practical requires a proper design of device structure, so that the voltage for charging a single electron is discrete and well separated (as compared to the noise level), as is the shift in threshold voltage caused by the storage of a single electron.

One of the two previous approaches to SEMM is to build the device in a tiny polysilicon strip (1). An electron percolation path in the strip forms the **channel**, and one of **polysilicon** grains near the conduction path acts as the floating gate. Such a structure intrinsically prevents precise control of the channel size, floating gate dimension, and tunnel barrier. The other approach is to replace the floating gate of conventional floating gate transistor memory with nanocrystal grains, while keeping the rest of the device unaltered (2). The size of the silicon nanocrystals and the tunnel barriers intrinsically have a broad distribution. Both approaches intend to alleviate the challenges in nanofabrication, but the statistical variations in their structures lead to large fluctuations in the shift of the threshold voltage and in the charging voltage, making them unsuitable for large-scale integration.

Here we present a SEMM in crystalline silicon that has a well-controlled dimension. Charging a single electron to the floating gate

leads, at room temperature, to a quantized shift in threshold voltage and a staircase relation between the shift and the charging voltage. Furthermore, the charging process is self-limited.

There are two key features of our SEMM (Fig. 1): (i) the channel width of silicon MOS field-effect transistor is narrower than the Debye screening length of a single electron and (ii) the floating gate is a nanoscale square (hence, it is called a dot) (3). Otherwise, the device is similar to an ordinary floating gate MOS memory. The narrow channel ensures that the storage of a single electron on the floating gate is sufficient to screen the entire channel (that is, the full channel width) from the potential on the control gate, which leads to a significant shift in threshold voltage. A small floating gate is used to significantly increase electron quantum energy (due to the small size) and electron charging energy (due to the small capacitance); hence, the threshold voltage shift and the charging voltage become discrete and well separated at room temperature. The control gate in our device is long, but the device's threshold is determined by the section where the floating gate is located.

In fabrication, an 11-nm-thick polysilicon film (for the floating gate) was deposited on a silicon-on-insulator wafer that had a 35-nm-thick top layer of crystalline silicon (for the **channel**). The **polysilicon** film and the silicon layer were separated by a layer of native oxide - 1 nm thick. The first level of electron beam lithography (EBL) and reactive ion etching (RIE) patterned the width of the floating gate and the narrow silicon channel, which is under the gate (that is, they are self-aligned). The initial channel width varied from 25 to 120 nm. A second level of EBL and RIE patterned the length of the floating gate, making it square (Fig. 2). An 18-nm-thick layer of oxide was then thermally grown, partially consuming the silicon, which reduced the thickness of the polysilicon dot by -9 nm and the lateral size of the dot and the width of the silicon channel by - 18 nm. A 22-nm-thick layer of oxide was deposited by plasmaenhanced chemical vapor deposition, making the total thickness of the control gate oxide 40 nm. Next, polysilicon was deposited, and the control gate was patterned to a length of 3 am, which covered the floating gate and part of the narrow channel. After making the final contacts, the devices were sintered in a forming gas to reduce the interface states. Many of the fabrications described here are similar to our previous work (4).

(Chart Omitted)

Captioned as: Fig. 1.

No tunnel oxide was intentionally grown between the **channel** and **polysilicon** floating gate. The reasons are twofold: to allow fast charging and to minimize the potential difference between the channel and the floating dot during the charging process, so that for a given charging voltage, the Coulomb blockade effect can regulate the number of electrons stored on the floating gate. In these devices, a potential barrier still exists between the channel and the floating gate, because of the grain boundary in polysilicon and the thin native oxide.

The devices were characterized at room temperature in a two-step process. First, a voltage pulse that was positive relative to the grounded source was applied to the control gate, while the drain voltage was maintained at 50 mV. This process caused electrons to tunnel from the channel to the floating gate. The drain current of the transistor was then measured as a function of the gate voltage (I-V) with a 50-mV source drain voltage, from which the threshold voltage (VMh) shift was obtained. A simple switching circuit was used to allow measurement of the I-V characteristics within 1 s after the completion of the charging process.

A SEMM that had an -10-nm-wide channel and an -7 nm by 7 nm square, 2-nm-thick floating gate-the smallest in our fabrication-was characterized under different charging voltages. The device dimension was estimated from measurements made with a scanning electron microscope and from the oxidation rate. However, self-limiting oxidation may have occurred (5), making it difficult to assess the exact size. We measured the I-V characteristics of the device after the control gate was pulsed by charging

voltages ranging from 0 to 14 V (Fig. 3). Although the charging voltage was continuous, the threshold voltage of the device (defined as the gate voltage at which the drain current reaches 100 pA) always made a discrete shift of 55 mV, and each shift corresponded to a charging voltage interval of -4 V (Fig. 4A). Moreover, for a given charging voltage, the threshold shift was self-limited; that is, the shift in threshold voltage was independent of the charging time (Fig. 4B). Because no tunnel oxide was intentionally added, the charge stored at the floating gate could be held for -5 s after the control gate potential was set back to the ground, and the threshold voltage of the device returned to its original value (leftmost trace in Fig. 3).

The behavior of the device can be explained by the single electron charging effect. Because the tunnel oxide between the **channel** and the floating gate was **thin**, the charging voltage dropped primarily between the control gate and the floating gate. To add one electron to the floating gate requires an increment of e/Cdg in charging voltage to be applied to the control gate, where e is the magnitude of a single electron charge and Cdg is the capacitance between the control gate and the floating gate (Fig. 5). The capacitance Cdg for the 7 nm by 7 nm floating gate and a 40-nm-thick layer of control oxide was about 4.4 x 10-20 F, giving a single electron charging voltage of 3.6 V, close to the experimental value of 4 V.

The shift in the SEMM's threshold voltage caused by one electron stored in the floating gate is given by AVth - e/(Cdg + Cf,,) (1)

Here Cfe, the fringe capacitance, accounts for the partial wrapping of the control gate around the channel so that the channel is only partially screened by the floating gate. For a conventional floating gate MOS memory, Cfs = 0, and AVt is reduced to the usual form *

Vch - e/Cdg. In our devices, Cag is about two orders of magnitude greater than Cde The value of Cfe can be estimated from the single electron Debye screen length (-70 nm) and the channel thickness (26 nm) in a parallel-capacitor model. For the control oxide thickness of 40 nm and the area of 70 nm by 26 nm, the Cfrg is about 2.5 X 10-is F, and hence, AVmh - 64 mV, which is again consistent with the experiment.

The self-limiting charging process can be explained by three facts: (i) The energy level spacing in the floating gate, which must be overcome to charge one more electron into the floating gate, is large compared with kBT (the thermal energy, Boltzmann's constant kB times temperature T) at room temperature. For a 7 nm by 7 nm silicon square embedded in SiO2, the quantum energy spacing is -30 meV, and the Coulomb energy spacing is 50 meV (assuming that the oxide layer between the dot and channel is 1 nm thick) (6); (ii) because the barrier layer is **thin**, the voltage drop between the **channel** and the floating gate is very small; and (iii) once an electron is added to the floating gate, the potential of the floating gate rises, further reducing the voltage difference between the channel and the floating gate and preventing another electron from tunneling into the floating gate. Therefore, for a fixed charging voltage, the charging process is self-regulated and stops once the floating gate is charged with a fixed number of electrons, leading to a threshold shift independent of charging time and a staircase relation between the charging voltage and the threshold shift.

(Chart Omitted)

Captioned as: Fig. 2.

(Graph Omitted)

Captioned as: Fig. 3.

(Graph Omitted)

Captioned as: Fig. 4.

The discrete threshold shift is not a result of interfacial traps. The threshold shifts due to the traps will not be equally spaced (because the charge will be trapped at different locations of the channel), and the charging process will be time dependent (7).

Despite the small floating gate and the low level of channel doping, the device has a good subthreshold slope of 108 mV per decade, because the

inversion layer induced by the control gate effectively acts as an ultrashallow source and drain for the device. This characteristic is also attributable to the low source and drain voltage.

As indicated by Eq. 1, the threshold voltage can be much larger than the present 55 mV if the thickness of the control gate oxide is increased or the fringing gate capacitance can be reduced. Also, if a thicker tunnel oxide is used between the channel and the floating gate, the charge on the floating gate can be held much longer than the current 5 s.

The SEMM should be investigated more thoroughly before being put into manufacturing. One of the most important questions to be studied is the effects of variations of device size and stray charges on the threshold voltage. Nevertheless, the SEMM presented here is orders of magnitude smaller than the conventional floating gate MOS memory, has properties that conventional memories do not have, and is a major step forward in taking advantage of single electron effects to build ultrasmall and ultrahigh density transistor memories.

(Chart Omitted)

Captioned as: Fig. 5. (A) Schematic

Footnote:

REFERENCES AND NOTES

Footnote:

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